**TSPi Plan Summary - Form SUMP**

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| Name | นางสาวปรีชญา ชูศรีทอง (PM)  นายกล้ายุทธ คลองแก้ว (P) | | | Date | | | | | | 29 ม.ค. 2565 | |
| Team | 4 | | | Instructor | | | | | | อ.อภิสิทธิ์ แสงใส | |
| Part/Level | System | | | Cycle | | | | | | 3 | |
| **Product Size** | | | **Plan** | | | |  | **Actual** | | | |
| Requirements pages (SRS) | | | 200 | | | |  | 274 | | | |
| เอกกสารการประชุม | | | 80 | | | |  | 107 | | | |
| High-level design pages (SDS) | | | 50 | | | |  | 62 | | | |
| Base LOC (B) (measured) | | | 0 | | | |  | 0 | | | |
| Deleted LOC (D) | | | 0 | | | |  | 0 | | | |
|  | | | (Estimated) | | | |  | (Counted) | | | |
| Modified LOC (M) | | | 0 | | | |  | 0 | | | |
|  | | | (Estimated) | | | |  | (Counted) | | | |
| Added LOC (A) | | | 0 | | | |  | 8,991 | | | |
|  | | | (N-M) | | | |  | (T-B+D-R) | | | |
| Reused LOC (R) | | | 0 | | | |  | 0 | | | |
|  | | | (Estimated) | | | |  | (Counted) | | | |
| Total New & Changed LOC (N) | | | 0 | | | |  | 0 | | | |
|  | | | (Estimated) | | | |  | (A+M) | | | |
| Total LOC (T) | | | 0 | | | |  | 8,991 | | | |
|  | | | (N+B-M-D+R) | | | |  | (Measured) | | | |
| Total New Reuse LOC | | | 0 | | | |  | 0 | | | |
| Estimated Object LOC (E) | | |  | | | |  |  | | | |
| Upper Prediction Interval (70%) | | |  | | | |  |  | | | |
| Lower Prediction Interval (70%) | | |  | | | |  |  | | | |
| **Time in Phase (hours)** | | **Plan** | | |  | **Actual** | | |  | | **Actual %** |
| Management and miscellaneous | | 60 | | |  | 60 | | |  | | 100 |
| Launch and strategy | | 10 | | |  | ไม่ทราบข้อมูล | | |  | | ไม่ทราบข้อมูล |
| Planning | | 187 | | |  | 176 | | |  | | 94.12 |
| Requirements | | 33 | | |  | 61.24 | | |  | | 185.58 |
| Test plan | | 6 | | |  | 4.25 | | |  | | 70.83 |
| Requirements review | | 23 | | |  | 20.40 | | |  | | 88.70 |
| High-level design | | 15.40 | | |  | 19.40 | | |  | | 125.97 |
| High-level design review | | 8.30 | | |  | 5.47 | | |  | | 35.52 |
| Implementation planning | | 79.10 | | |  | 76.40 | | |  | | 194.31 |
| Code | | 81.2 | | |  | 88.46 | | |  | | 108.94 |
| Code review | | 23.3 | | |  | 20.06 | | |  | | 86.09 |
| Compile | | ไม่ทราบข้อมูล | | |  | ไม่ทราบข้อมูล | | |  | | ไม่ทราบข้อมูล |
| Unit test | | ไม่ทราบข้อมูล | | |  | ไม่ทราบข้อมูล | | |  | | ไม่ทราบข้อมูล |
| Build and integration | | 147.55 | | |  | 156.26 | | |  | | 105.9 |
| System test | | 4 | | |  | ไม่ทราบข้อมูล | | |  | | ไม่ทราบข้อมูล |
| Documentation | | 308.50 | | |  | 363.39 | | |  | | 117.79 |
| Postmortem | | 180 | | |  | - | | |  | | ไม่ทราบข้อมูล |
| Total | | 1166.35 | | |  | 1051.33 | | |  | | 90.14 |
| Total Time UPI (70%) | | - | | |  |  | | |  | |  |
| Total Time LPI (70%) | | - | | |  |  | | |  | |  |

**TSPi Plan Summary - Form SUMP (continued)**

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| Name | นางสาวปรีชญา ชูศรีทอง (PM)  นายกล้ายุทธ คลองแก้ว (P) | Date | 29 ม.ค. 2565 |
| Team | 4 | Instructor | อ.อภิสิทธิ์ แสงใส |
| Part/Level | System | Cycle | 3 |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Defects Injected** | **Plan** |  | **Actual** |  | **Actual %** |
| Strategy and Planning | 0 |  | 0 |  | 0 |
| Requirements | 0 |  | 0 |  | 0 |
| System test plan | 0 |  | 0 |  | 0 |
| Requirements inspection | 0 |  | 0 |  | 0 |
| High-level design | 0 |  | 1 |  | 0 |
| Integration test plan | 0 |  | 0 |  | 0 |
| High-level design inspection | 0 |  | 0 |  | 0 |
| Detailed design | 0 |  | 0 |  | 0 |
| Detailed design review | 0 |  | 0 |  | 0 |
| Test development | 0 |  | 0 |  | 0 |
| Detailed design inspection | 0 |  | 0 |  | 0 |
| Code | 80 |  | 75 |  | 93.45 |
| Code review | 0 |  | 0 |  | 0 |
| Compile | 0 |  | 0 |  | 0 |
| Code inspection | 0 |  | 0 |  | 0 |
| Unit Test | 0 |  | 1 |  | 0 |
| Build and integration | 0 |  | 0 |  | 0 |
| System test | 0 |  | 0 |  | 0 |
| Total Development | 80 |  | 77 |  |  |
| **Defects Removed** | **Plan** |  | **Actual** |  | **Actual %** |
| Strategy and Planning | 0 |  | 0 |  | 0 |
| Requirements | 0 |  | 0 |  | 0 |
| System test plan | 0 |  | 0 |  | 0 |
| Requirements inspection | 0 |  | 0 |  | 0 |
| High-level design | 0 |  | 0 |  | 0 |
| Integration test plan | 0 |  | 0 |  | 0 |
| High-level design inspection | 0 |  | 0 |  | 0 |
| Detailed design | 0 |  | 0 |  | 0 |
| Detailed design review | 0 |  | 0 |  | 0 |
| Test development | 0 |  | 0 |  | 0 |
| Detailed design inspection | 0 |  | 0 |  | 0 |
| Code | 0 |  | 0 |  | 0 |
| Code review | 0 |  | 13 |  | หาค่าไม่ได้ |
| Compile | 70 |  | 63 |  | 90 |
| Code inspection | 0 |  | 0 |  | 0 |
| Unit Test | 0 |  | 1 |  | 0 |
| Build and integration | 0 |  | 0 |  | 0 |
| System test | 0 |  | 0 |  | 0 |
| Total Development | 70 |  | 77 |  |  |

**TSPi Plan Summary Instructions - Form SUMP**

|  |  |
| --- | --- |
| **Purpose** | * This form holds plan and actual data for program parts or assemblies. |
| **General** | * An assembly could be a system with multiple products, a product with multiple components, or a component with multiple modules. * A part could be a module, component, or product. * Note: the lowest-level parts or modules typically have no system-level data, such as requirements, high-level design, or system test. |
| **Using the TSPi Tool** | When using the TSPi tool, the plan values are automatically generated.   * The time and size data are computed from the TASK and SUMS forms. * The defect values are automatically generated during the quality planning process (SUMQ).   The actual values are also automatically generated by the TSPi tool.   * Time and size values come from the LOGT, TASK, and SUMS forms. * Defect data come from the LOGD forms.   When not using the TSPi tool, follow the instructions below. |
| **Header** | * Enter your name, date, team name, and instructor's name. * Name the part or assembly and its level. * Enter the cycle number. |
| **Columns** | * Plan: This column holds the part or assembly plan data. * Actual: For assemblies, this column holds the sum of the actual data for the parts of the assembly (at the lowest level, the modules). |
| **Product Size** | * For text and designs, enter only the new and changed size data. * For program parts or assemblies, enter all the indicated LOC data. * Obtain the data from the SUMS form. |
| **Time in Phase** | * Enter estimated and actual time by phase. * For parts, obtain these data from the TASK forms for those parts. * For assemblies, obtain the part-level time data from the totals on the SUMT form and the assembly-level data from the assembly-level TASK form. * For example, HLD time would come from the assembly TASK form while total part unit test time would come from the SUMT form. * Actual %: Enter the percent of the actual development time by phase. |
| **Defects Injected** | * Enter estimated and actual defects injected by phase. * Enter the defect estimates while producing the quality plan. * For parts, obtain actual data from the LOGD forms for those parts. * For assemblies, get part-level defect data from the totals of the SUMDI form and assembly-level data from the assembly LOGD form. * For example, HLD defects would come from the assembly LOGD form while the total part coding defects would come from the SUMDI form. * Actual %: Enter the percent of the actual defects injected by phase. |
| **Defects Removed** | * Enter estimated and actual defects removed by phase. * Enter the defect estimates while producing the quality plan. * For parts, obtain actaul data from the LOGD forms for those parts. * For assemblies, obtain part-level defect data from the totals of the SUMDR form and assembly-level data from the assembly LOGD form. * For example, HLD review defects would come from the assembly LOGD form while the total part code review defects would come from the SUMDR form. * Actual %: Enter the percent of the actual defects removed by phase. |